USN | | | | | | | | | | |

10CS74

Seventh Semester B.E. Degree Examination, June/July 2014
Advanced Compute Architectures

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO question from each part.***

PART – A

1 a. Define computer architecture. List and explain four important technologies, which lead to the improvements in computer system. **(10 Marks)**

b. Find the number of dies per 300 mm (30cm) wafer for a die that is 1.5 cm on a side. **(02 Marks)**

c. Define Amdahls law. Derive an expression for CPU clock as a function of instruction count, clock per instruction and clock cycle time. **(08 Marks)**

2 a. List three major hurdles of pipelining. Explain the concept of minimizing data hazards stalls by forwarding. **(10 Marks)**

b. Briefly explain how the MIPS instructions can be implemented in at most five clock cycles. **(05 Marks)**

c. List and explain five different ways of classifying exceptions in a computer system. **(05 Marks)**

3 a. What is instruction level parallelism? Explain control dependence using code fragment. **(08 Marks)**

b. Explain the states in 2 – bit prediction scheme used for dynamic Brach prediction. **(06 Marks)**

c. With a neat diagram, explain the basic structure of a MIPS floating pint unit using Tomasulo's algorithm. **(06 Marks)**

4 a. With a neat diagram, explain the four steps involved in executing instructions using hardware based speculation. **(10 Marks)**

b. What is branch target buffer? With a neat diagram, explain the steps when using branch target buffer for a simple five stage pipeline. **(10 Marks)**

PART – B

5 a. To achieve a speedup of 80 with 100 processors what fraction of the original computation can be sequential? **(04 Marks)**

b. Explain the two cache coherence protocols used for enforcing coherence. **(06 Marks)**

c. Explain directory based cache coherence for a distributed memory multiprocessor system along with the state transition diagram. **(10 Marks)**

6 a. List and explain any four basic cache optimization techniques. **(10 Marks)**

b. With a neat diagram, explain the translation buffer of fast address translation. **(10 Marks)**

7 a. List any five advanced optimizations of cache performance and explain briefly the complier

b. optimization to reduce miss rate. **(10 Marks)**

Explain briefly how memory protection is enforced via virtual memory and via virtual machines. **(10 Marks)**

8 a. Explain the architecture of IA64 intel processor and also the prediction and speculation support provided. **(10 Marks)**

b. Write short notes on benchmarks. **(05 Marks)**

c. Explain the internal organization of 64M bit DRAM. **(05 Marks)**

* * * * *